

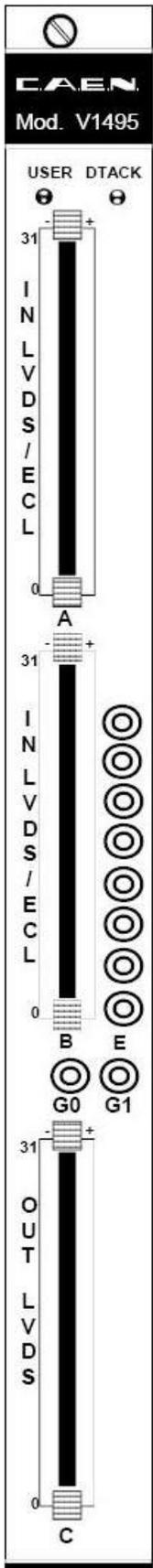
## CAEN V1495 Based Trigger Module and Laser Pulse Controller

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*Physics experiments use triggers as one piece of the data acquisition system. The triggers designed in this paper use a Caen V1495. The Caen V1495 features a field programmable gate array (FPGA) in the Cyclone family designed by Altera Inc. The designs detailed in this paper are a machine protection system for a laser beam and a multiplicity trigger for the Darkside-50 project.*

FPGA's are used as the base for the trigger systems due to their flexibility. As the name implies they are "field-programmable" and therefore can have the specifications changed at any time. The FPGA configuration is specified using Very high speed Integrated Hardware Design Language (VHDL) or schematics of logic design. For the purpose of legibility, from the Block Design File (BDF) are featured throughout our design work. The BDF is a visual representation of both the behavior and the structure of the logic circuits. Other aspects of design such as timing and pin layout are handled by the Quartus software designed by Altera which is specifically designed to handle the FPGA devices including the Cyclone chip used by the CAEN V1495.

The CAEN V1495 front end features three 32 channel ribbon cables. The slots designated A and B are designated inputs and C is a designated output. The ribbon cable settings are hardwired and not adjustable. In addition to the ribbon cables, a daughter card with eight NIM outputs, plugged in the E extension slot, are in vertical succession next to the B ribbon cable. Two NIM inputs are located beneath B and E, designated G.



There are two applications for which the CAEN V1495 has been used. Darkside-50 uses a CAEN V1495 as a multiplicity trigger and at the New Muon Laboratory (NML) it is used as part of the Machine Protection System (MPS) as the Laser Pulse Controller (LPC). The front end was used for different purposes for each project but there was no change in the mezzanine cards. There are two empty slots in which additional mezzanine cards could be placed at a later date before final installation.

The multiplicity trigger built for Darkside-50 included inputs for thirty eight channels and a trigger output. The logic built for Darkside-50 includes a coincidence time window, inhibitor time window, and record signal keeping. There are also additional needs that need to be addressed, algorithms for comparing Signal 1 and Signal 2, signal channel record keeping and additional signals as determined by the research group.

In order to address the need for thirty eight channels of input ribbon cable inputs A and B are utilized. Both contain input channels over all of their thirty two channels. These channels drive the trigger and are subject to user controlled multiplicity setting and masking settings. Four registers on the FPGA are utilized for the masking of the channels and one is utilized for the multiplicity setting. These register decisions are decided according to the CAEN V1495 manual.

Within the trigger build is the multiplicity setting. In addition to requiring a specific number of channels to drive the trigger, there are requirements on the amount of time between triggers and the number of triggers allowed within a specific time window. All of these settings are controllable via the register settings on the FPGA.

Figure 1: CAEN V1495 Front End

Reg. Name	Address	Data Sizing	Access	Notes	Units
CC	0x28	D16	RW	Adjusts the multiplicity level	$N + 1$ signals
PW	0x2a	D16	RW	Width of the trigger inhibitor	
MSK_A_L	0x30	D16	RW	Mask select for A_Low inputs	$N$ bits masked
MSK_A_H	0x32	D16	RW	Mask select for A_High inputs	$N$ bits masked
MSK_B_L	0x38	D16	RW	Mask select for B_Low inputs	$N$ bits masked
MSK_B_H	0x3a	D16	RW	Mask select for B_High inputs	$N$ bits masked
TW	0x1a	D16	RW	Coincidence time window	

Table 1: Darkside-50 Register List

The design also contains record keeping for the 38 LVDS signals. The incoming hit signals are sampled in 4 ns intervals and then stretched to fit in 16 ns clock domain. The hits are stored in the RAM located on the V1495. Upon receiving of input trigger, the RAM filling is stopped after a delay controlled by a register. The records are kept in the memory registers beginning at 0x200. There is a lot of work still to be done with this feature. Specifically the

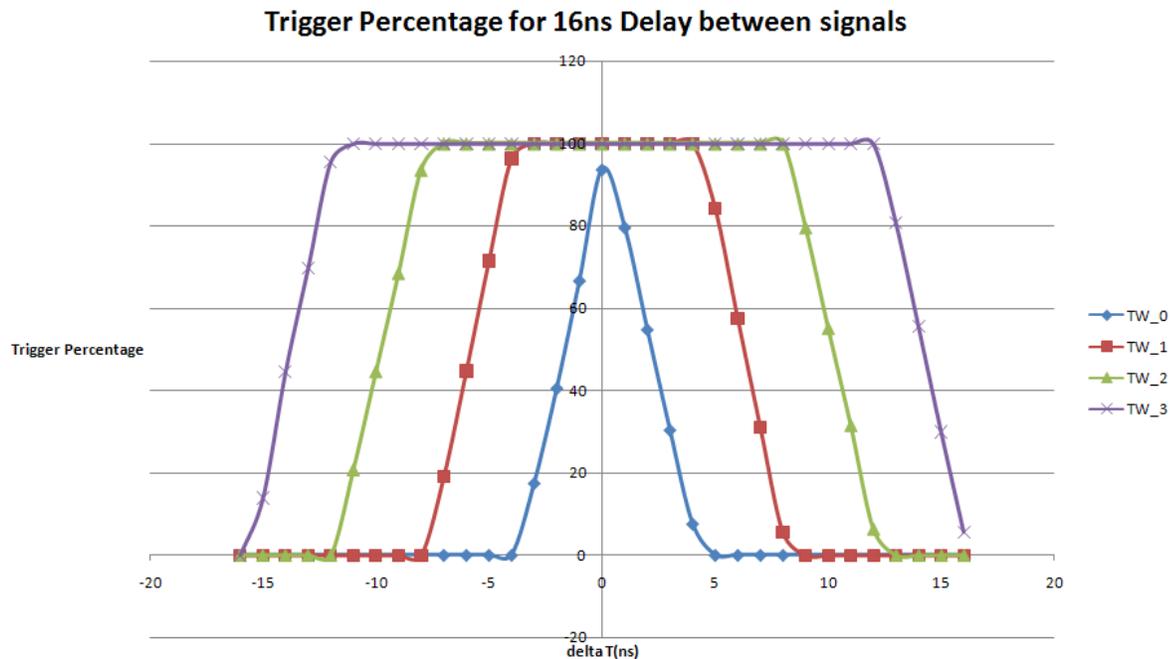
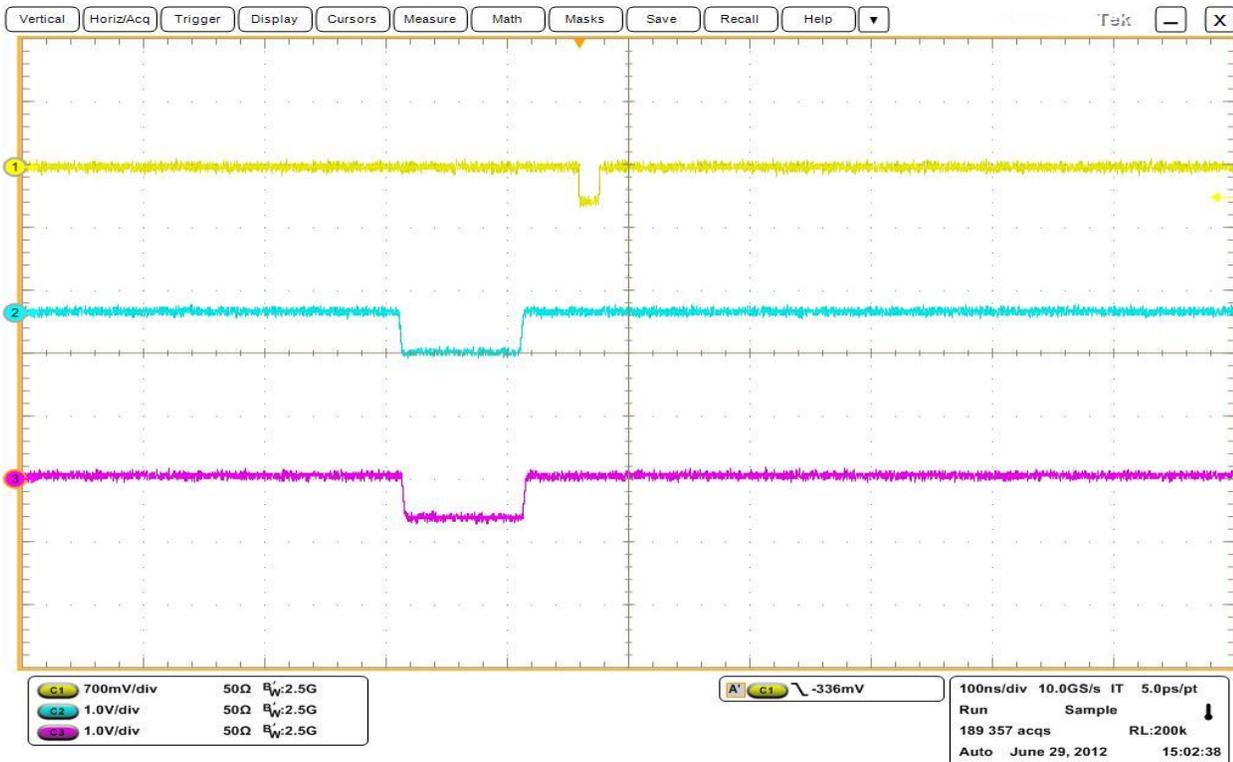


Figure 2: Trigger percentage compared to delay between signals for time window register 1-4

record of how many hits needs to be supplemented by a record of the channels on which the signals come in on.

In addition to the firmware design for Darkside-50 work was done testing how the design behaved and what may be needed in order to improve it. Looking at how the trigger percentage was affected by changing time windows and delay settings was particularly useful. The test showed that while all of the settings we had designed worked, there was a loss of triggers when the delays between signals neared the limiting time window.

There was a test implemented after every change in the design in order to insure that the firmware was working. Our results showed that we had successfully implemented a trigger than had user controlled settings on multiplicity settings, a trigger inhibitor window, a coincidence time window, the ability to mask all channels, and record keeping within the RAM.



*Figure 3: Channels 2 & 3 are generated pulses mimicking the LVDS signal. Channel 1 is the trigger created by the V1495 board. The trigger has a multiplicity requirement set by the user.*

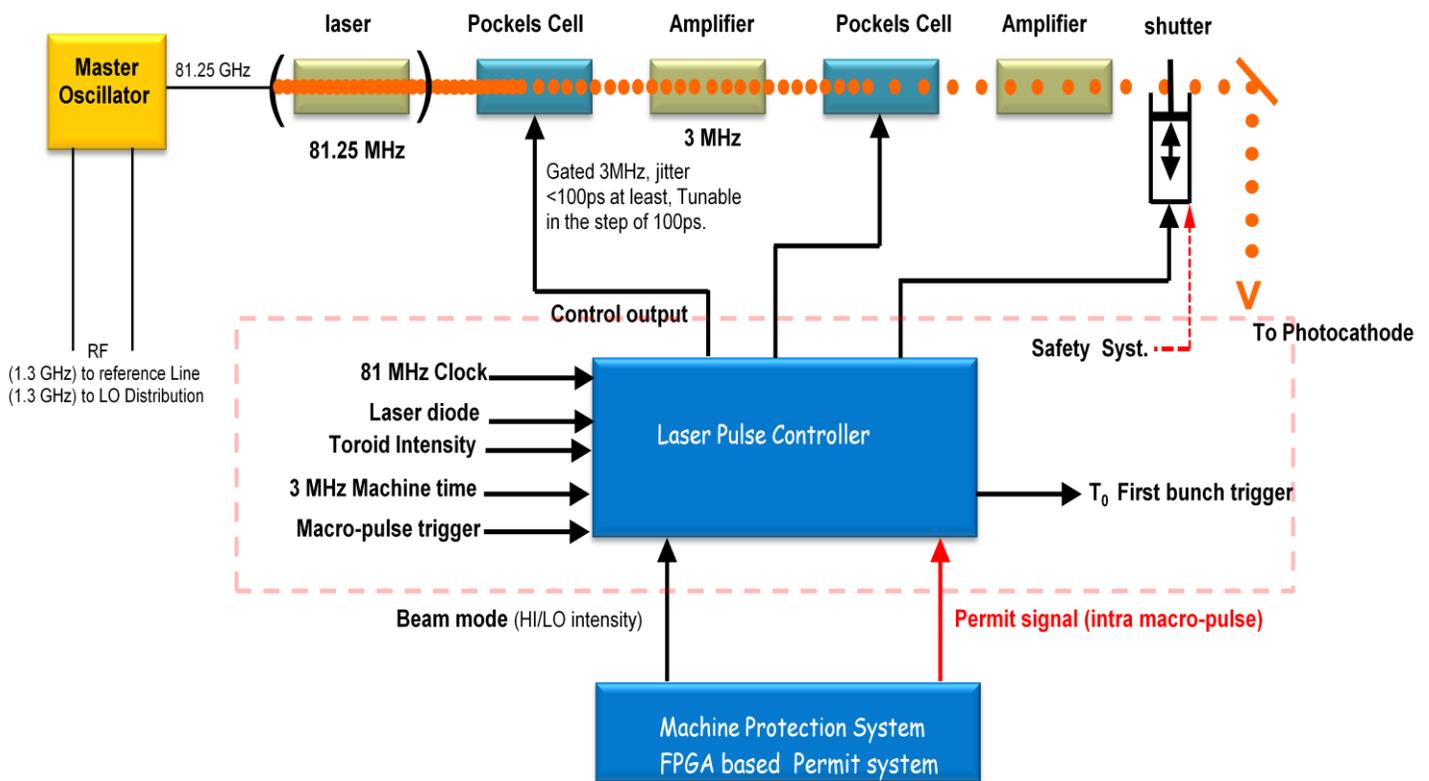


Figure 4: Design for the laser system including computer system. The portion inside the dashed rectangle is the portion addressed in this paper.

The LPC for the NML laser room uses the CAEN V1495 in different ways. As seen in Fig. 4 the LPC is designed to block the pockels cell based on pulse kickers while the MPS is in an alarm state. The LPC will also enforce the limit on the number of bunches as given by the selected beam mode. The LPC, when requested by the MPS, will close the laser shutter. This may happen when there is no valid operational mode or when some combination of loss monitors exceed thresholds which trigger a dump condition. Lastly the LPC must monitor the quantum efficiency of the gun/laser system.

The front end utilizes A and B as designated inputs and C as a designated output. While these are the settings for the front end only A includes signals that will be implemented in the final design. The first and last channels on A are used for the board driving signal and the reduced run condition signal respectively. E is designated as an output NIM signal and G is

designated as an input NIM signal. E's first channel is the laser enable signal and the second channel is the trigger for the first macro pulse. There will be more signals needed in the final implementation of the firmware that have not been designed yet. This design is the same as the design for Darkside-50 in the fact that it also has two open mezzanine slots on the board.

As in Darkside-50 a series of registers control the settings for the firmware. These settings are user readable and writable with the exception of the two registers determining what kind of signals the board can receive. Details of all the control registers are in *Table 2*. Unlike Darkside-50, which lacks any user interface, for the LPC Rich Neswold has designed an ACNET interface. This interface displays the registers that are user controllable in a user friendly way.

Reg. Name	Address	Data Sizing	Access	Notes	Units
ND_ST	0x28	D16	RW	Controls the delay of Gate TK	$n * \left(\frac{1}{3MHz}\right)$
ND_FP	0x2a	D16	RW	Controls the delay of the first pulse output from E_DOUT[1]	$n * \left(\frac{1}{3MHz}\right)$
NP	0x30	D16	RW	Sets the number of pulses to one less than that of which they are in normal run conditions	Pulses (+1 added automatically)
NPlow	0x32	D16	RW	Sets the number of pulses to one less than that of which they are in reduced run conditions	Pulses (+1 added automatically)
ND	0x38	D16	RW	Controls the fine tuning for the delay of GateTK output using E_DOUT[0]	$n * \left(\frac{1}{324MHz}\right)$
NW	0x3a	D16	RW	Controls the pulse width of GateTK output	$n * \left(\frac{1}{324MHz}\right)$
C_Reg	0x1a	D16	RW	Selects the speed of the macro pulse trigger	$20MHz/2^{n+22}$ Except when the register is set to 0. Then it becomes $/2^7$
G_Control	0x22	D16	R	[bit0=mezzanine output level]: '0': TTL '1': NIM	N/A
E_Control_L	0x2c	D16	R	[bit0=mezzanine output level]: '0': TTL '1': NIM	N/A

Table 2: LPC Register Designations

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PB N8 NML Misc<NoSets>
N8                               SET      D/A    A/D    Com-U ♦PTools♦
-<FTP>+ *SA♦ X-A/D X=TIME      Y=U:GRWD45,E UVB02 ,E UVB03 ,E UVB04
COMMAND ---X Eng-U I= 0      I=-1      , -20      , -40      , -20
-< 7>+ Once AUTO F= 4      F= 1      , 20      , 40      , 20
MISC      klystron.. cryo deg c cryo deg k windowtest ..ding...

-N:LGPRPW      Laser gun gate delay      .667      uS
-N:LGPRD1      Laser gun 1st pulse dly    .333      uS

-N:LGPRNP      Laser gun active pulses    20      puls
-N:LGPRNL      Laser gun low pulses       8      puls

-N:LGPRD2      Laser gun GateTK delay     6.173     nS
-N:LGPRNW      Laser gun GateTK width     77.16     nS

-N:LGPRPT      Laser gun pulse trig spd   0      N

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Figure 5: ACNET User control interface

Unlike with Darkside-50 the LPC was installed in its final location. At this location there were two different clock signals needed for the board. These signals were tested and determined to be a 3 MHz PECL signal that is then converted into a TTL signal and an 81 MHz sin wave signal. This was what was expected to be installed but it was not expected that this 81 MHz signal would not drive the board. This issue is still being resolved.

The LPC design was tested thoroughly to insure that all of the designs in the firmware are working as expected. Again, as with the Darkside project, there are many things still needing completion. The LPC to date includes, a delay of macro pulses from the initiation of the pulse as

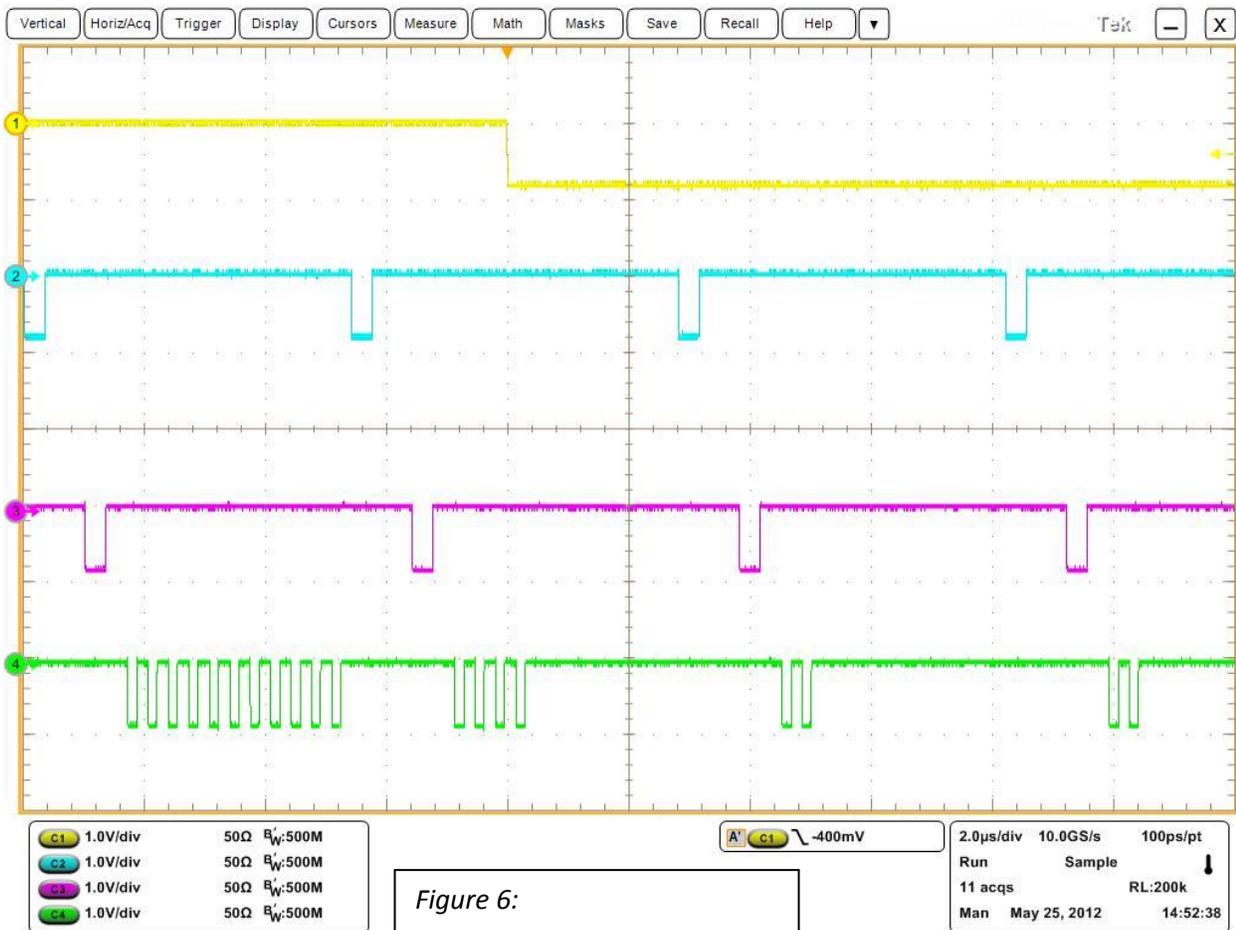


Figure 6:

Ch. 1: Reduced Run Condition

Ch. 2: First Pulse Trigger

Ch. 3: Generated First Pulse

Ch. 4: Pulse Control Signal

well as a delay between the trigger and the pulse, a fine tuning adjustment for the aforementioned delay, a control of the pulse width, a reduced run condition trigger, and control of the number of pulses in both reduced and normal run conditions.

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